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EXAMINER	
SAVLA, ARPAN P	

ART UNIT	PAPER NUMBER
2185	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/715,595	KUSUMOTO ET AL.	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 4-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 4-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office action is in response to Applicant's communication filed July 19, 2006 in response to the Office action dated January 20, 2006. Claims 1, 6-8, 15-16, and 19-21 have been amended. Claims 2-3 have been canceled. New claims 28-29 have been added. Claims 1 and 4-29 are pending in this application.

OBJECTIONS

Specification

1. In view of Applicant's amendment, the objections to the specification have been withdrawn.

REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 112

2. In view of Applicant's amendment, the 112 rejections to **claims 2-3** have been withdrawn.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 15-17, 19-25, and 29 are rejected under 35 U.S.C. 103(a) as being obvious over Yamada et al. (U.S. Patent 5,950,222) in view of Iwata (U.S. Patent 5,881,295).

5. **As per claim 15**, Yamada discloses a microcomputer comprising:

a nonvolatile memory including at least a first storage area and a second storage area in which delete and write of data is electrically performed independently (col. 3, lines 12-19; Fig. 1, element 1); *It should be noted that "EEPROM" is analogous to "nonvolatile memory", "region A" is analogous to "first storage area", and "region B" is analogous to "second storage area."*

wherein a plurality of interrupt vectors indicating respective storage places of a plurality of interrupt programs executed upon requesting of an interrupt is stored in the first storage area (col. 8, lines 25-29; Fig. 8, elements (31-1)~(31-n));

and a plurality of alternate interrupt vectors corresponding to the respective interrupt vectors is stored in the second storage area (col. 8, lines 22-25; Fig. 8, elements (30-1)~(30-n));

a central processing unit that has a mechanism to access the nonvolatile memory (col. 3, lines 19-23 and 28-29; Fig. 1, element 2).

Yamada does not expressly disclose a flag indicating that the first storage area is not accessible;

and a conversion circuit that includes a first pair of registers for setting a first address range and a second pair of registers for setting a second address range, and

that, when an address within the first range is accessed by the central processing unit, performs address conversion based on a state of the flag, to convert the first address range to the second address range.

Iwata discloses a flag indicating that the first storage area is not accessible (col. 9, lines 51-55 and 58-61; col. 10, lines 50-58; Fig. 1, element 18); *It should be noted that when the built-in ROM is in boot or user program mode the contents of the built-in ROM are not accessible. MS0 and MS1 are flags indicating whether the built-in ROM is in boot or user program mode respectively, therefore, MS0 and MS1 are also flags that indicate the built-in ROM is not accessible.*

and a conversion circuit that includes a first pair of registers for setting a first address range and a second pair of registers for setting a second address range, and that, when an address within the first range is accessed by the central processing unit, performs address conversion based on a state of the flag, to convert the first address range to the second address range (col. 14, lines 6-15; col. 23, line 60 – col. 24, line 13; Fig. 5; Fig. 19). *It should be noted that the "vector address storage area A-V" is analogous to the "first address range", the "vector address storage area B-V" is analogous to the "second address range", registers "PEREG" and "MBREG1" are analogous to the "first pair of registers for setting a first address range", and registers "PEREG" and "MBREG2" are analogous to the "second pair of registers for setting a second address range."*

Yamada and Iwata are analogous because they are from the same field of endeavor, that being microcomputers.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Iwata's conversion circuit within Yamada's microcomputer.

The motivation for doing so would have been to improve the safety of a system during on-board programming of a program memory (Iwata, col. 3, lines 25-27). Also, another motivation for doing so would have been to provide additional safety by preventing a microcomputer from running away and from being damaged even when an interrupt handling or exception handling is requested during on-board programming of the above program memory (Iwata, col. 3, lines 31-34).

Therefore, it would have been obvious to combine Yamada and Iwata for the benefit of obtaining the invention as specified in claim 15.

6. **As per claim 16**, the combination of Yamada/Iwata discloses the conversion circuit performs address conversion individually for a plurality of address ranges, each of the plurality of address ranges including each of the interrupt vectors (Iwata, col. 11, lines 34-38).

7. **As per claim 17**, the combination of Yamada/Iwata discloses the conversion circuit comprises hardware that performs a predetermined conversion operation (Iwata, col. 11, line 65 – col. 12, line 21; Fig. 3).

8. **As per claim 19**, the combination of Yamada/Iwata discloses the nonvolatile memory, the central processing unit, the flag, and the conversion circuit are integrated on a same semiconductor chip (Iwata, col. 6, lines 46-50; Fig. 1, element 30).

9. **As per claim 20**, the combination of Yamada/Iwata discloses the interrupt program is stored in the first storage area, the interrupt vector indicates a start address

of the interrupt program, the alternate interrupt program that is executed instead of the interrupt program is stored in the second storage area, and the alternate interrupt vector indicates a start address of the alternate interrupt program (Yamada, col. 8, lines 14-29; Fig. 1, element 1). *It should be noted that it is inherently required an interrupt vector store the starting address of it's corresponding interrupt handler routine (interrupt program).*

10. **As per claim 21**, the combination of Yamada/Iwata discloses the interrupt program is stored in the second storage area, and the interrupt vector and the alternate interrupt vector store a start address of the interrupt program (Iwata, col. 17, lines 50-58; col. 17, line 66 – col. 18, line 3; Fig. 1, element 13). *It should be noted that "built-in RAM" is analogous to "second storage area", "NMI handling routine RB" is analogous to "interrupt program", "vector address NMIA" is analogous to "interrupt vector", and "vector address NMIB" is analogous to "alternate interrupt vector." It should also be noted that when in user program mode or boot mode both NMIA and NMIB, which are stored in the built-in RAM, access NMI handling routine RB.*

11. **As per claim 22**, the combination of Yamada/Iwata discloses a main program is stored in the first storage area (Iwata, col. 9, lines 8-9; Fig. 1, element 18). *It should be noted that "built-in ROM" is analogous to "first storage area."*

12. **As per claim 23**, the combination of Yamada/Iwata discloses a main program is stored in the first storage area (Iwata, col. 9, lines 8-9; Fig. 1, element 18).

13. **As per claim 24**, the combination of Yamada/Iwata discloses a main program is stored in the second storage area (Iwata, col. 10, lines 15-17; Fig. 1, element 13).

14. **As per claim 29**, Yamada discloses a microcomputer comprising:

a nonvolatile memory including at least a first storage area and a second storage area in which delete and write of data is electrically performed independently (col. 3, lines 12-19; Fig. 1, element 1); *See citation note for the similar limitation in claim 15 above.*

a central processing unit that has a mechanism to access the nonvolatile memory (col. 3, lines 19-23 and 28-29; Fig. 1, element 2).

Yamada does not expressly disclose a flag indicating that the first storage area is not accessible;

and a conversion circuit that, based on a state of the flag, converts an address indicating a storage place of an interrupt vector that is accessed by the central processing unit into an address indicating a storage place of a corresponding alternate interrupt vector.

Iwata discloses a flag indicating that the first storage area is not accessible (col. 9, lines 51-55 and 58-61; col. 10, lines 50-58; Fig. 1, element 18); *See the citation note for the similar limitation in claim 15 above.*

and a conversion circuit that, based on a state of the flag, converts an address indicating a storage place of an interrupt vector that is accessed by the central processing unit into an address indicating a storage place of a corresponding alternate interrupt vector (col. 14, lines 6-15; Fig. 5).

Yamada and Iwata are analogous because they are from the same field of endeavor, that being microcomputers.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Iwata's conversion circuit within Yamada's microcomputer.

The motivation for doing so would have been to improve the safety of a system during on-board programming of a program memory (Iwata, col. 3, lines 25-27). Also, another motivation for doing so would have been to provide additional safety by preventing a microcomputer from running away and from being damaged even when an interrupt handling or exception handling is requested during on-board programming of the above program memory (Iwata, col. 3, lines 31-34).

Therefore, it would have been obvious to combine Yamada and Iwata for the benefit of obtaining the invention as specified in claim 29.

15. Claims 1, 4, and 6-12 are rejected under 35 U.S.C. 103(a) as being obvious over Yamada et al. (U.S. Patent 5,950,222) in view of Iwata (U.S. Patent 5,881,295) and further in view of Hashimoto (U.S. Patent 6,654,839).

16. **As per claim 1**, Yamada discloses a microcomputer comprising:

a nonvolatile memory including at least a first storage area and a second storage area in which delete and write of data is electrically performed independently (col. 3, lines 12-19; Fig. 1, element 1); *See citation note for the similar limitation in claim 15 above.*

wherein a plurality of interrupt vectors indicating respective storage places of a plurality of interrupt programs executed upon requesting of an interrupt is stored in the first storage area (col. 8, lines 25-29; Fig. 8, elements (31-1)~(31-n));

and a plurality of alternate interrupt vectors corresponding to the respective interrupt vectors is stored in the second storage area (col. 8, lines 22-25; Fig. 8, elements (30-1)~(30-n));

a central processing unit that has a mechanism to access the nonvolatile memory (col. 3, lines 19-23 and 28-29; Fig. 1, element 2).

Yamada does not expressly disclose a flag indicating that the first storage area is not accessible;

and a conversion circuit that includes a plurality of registers to which a plurality of addresses indicating respective storage places of the alternate interrupt vectors are set, and that, based on a state of the flag, converts a first address indicating a storage place of the interrupt vector that is accessed by the central processing unit into a second address indicating a storage place of the corresponding alternate interrupt vector by outputting the second address from one of the registers corresponding to the first address.

Iwata discloses a flag indicating that the first storage area is not accessible (col. 9, lines 51-55 and 58-61; col. 10, lines 50-58; Fig. 1, element 18); *See the citation note for the similar limitation in claim 1 above.*

and a conversion circuit that includes a plurality of registers, based on a state of the flag, converts a first address indicating a storage place of the interrupt vector that is accessed by the central processing unit into a second address indicating a storage place of the corresponding alternate interrupt vector (col. 14, lines 6-15; col. 23, lines 60-63; Fig. 5; Fig. 19).

Yamada and Iwata are analogous because they are from the same field of endeavor, that being microcomputers.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Iwata's conversion circuit within Yamada's microcomputer.

The motivation for doing so would have been to improve the safety of a system during on-board programming of a program memory (Iwata, col. 3, lines 25-27). Also, another motivation for doing so would have been to provide additional safety by preventing a microcomputer from running away and from being damaged even when an interrupt handling or exception handling is requested during on-board programming of the above program memory (Iwata, col. 3, lines 31-34).

The combination of Yamada/Iwata does expressly disclose a conversion circuit that includes a plurality of registers to which a plurality of addresses indicating respective storage places of the alternate interrupt vectors are set, and that, based on a state of the flag, converts a first address indicating a storage place of the interrupt vector that is accessed by the central processing unit into a second address indicating a storage place of the corresponding alternate interrupt vector by outputting the second address from one of the registers corresponding to the first address.

Hashimoto discloses a plurality of registers to which a plurality of addresses indicating respective storage places of the alternate interrupt vectors are set, that outputs the second address from one of the registers corresponding to the first address (col. 6, lines 41-45, 53-59, and 63-65; Fig. 5, elements 50, 54, and the "VTA (vector

table address)"). *It should be noted that the "base register" and the "interrupt factor register" are analogous to the "plurality of registers."*

The combination of Yamada/Iwata and Hashimoto are analogous because they are from the same field of endeavor, that being microcomputers.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Hashimoto's registers within Yamada/Iwata's microcomputer.

The motivation for doing so would have been to make the device more convenient to the user, by enabling the storage of a series of interrupt vectors at addresses within a memory as desired by the user (Hashimoto, col. 3, lines 4-6).

Therefore, it would have been obvious to combine Yamada, Iwata, and Hashimoto for the benefit of obtaining the invention as specified in claim 1.

17. **As per claim 4**, the combination of Yamada/Iwata/Hashimoto discloses the conversion circuit comprises hardware that performs a predetermined conversion operation (Iwata, col. 14, lines 19-35; Fig. 5).

18. **As per claim 6**, the combination of Yamada/Iwata/Hashimoto discloses the nonvolatile memory, the central processing unit, the flag, and the interrupt vector address conversion circuit are integrated on a same semiconductor chip (Iwata, col. 6, lines 46-50; Fig. 1, element 30).

19. **As per claim 7**, the combination of Yamada/Iwata/Hashimoto discloses the interrupt program is stored in the first storage area, the interrupt vector indicates a start address of the interrupt program, the alternate interrupt program that is executed

instead of the interrupt program is stored in the second storage area, and the alternate interrupt vector indicates a start address of the alternate interrupt program (Yamada, col. 8, lines 14-29; Fig. 1, element 1). *See the citation note for claim 20 above.*

20. **As per claim 8**, the combination of Yamada/Iwata/Hashimoto discloses the interrupt program is stored in the second storage area, and the interrupt vector and the alternate interrupt vector indicate a start address of the interrupt program (Iwata, col. 17, lines 50-58; col. 17, line 66 – col. 18, line 3; Fig. 1, element 13). *See the citation note for claim 21 above.*

21. **As per claim 9**, the combination of Yamada/Iwata/Hashimoto discloses a main program is stored in the first storage area (Iwata, col. 9, lines 8-9; Fig. 1, element 18). *See the citation note for claim 22 above.*

22. **As per claim 10**, the combination of Yamada/Iwata/Hashimoto discloses a main program is stored in the first storage area (Iwata, col. 9, lines 8-9; Fig. 1, element 18).

23. **As per claim 11**, the combination of Yamada/Iwata/Hashimoto discloses a main program is stored in the second storage area (Iwata, col. 10, lines 15-17; Fig. 1, element 13).

24. **As per claim 12**, the combination of Yamada/Iwata/Hashimoto discloses a main program is stored in the second storage area (Iwata, col. 10, lines 15-17; Fig. 1, element 13).

25. Claim 28 is rejected under 35 U.S.C. 103(a) as being obvious over Yamada et al. (U.S. Patent 5,950,222) in view of Iwata (U.S. Patent 5,881,295) and further in view of Yoshioka et al. (U.S. Patent 6,038,661).

26. Yamada discloses a microcomputer comprising:

a nonvolatile memory including at least a first storage area and a second storage area in which delete and write of data is electrically performed independently (col. 3, lines 12-19; Fig. 1, element 1); *See citation note for the similar limitation in claim 15 above.*

wherein a plurality of interrupt vectors indicating respective storage places of a plurality of interrupt programs executed upon requesting of an interrupt is stored in the first storage area (col. 8, lines 25-29; Fig. 8, elements (31-1)~(31-n));

and a plurality of alternate interrupt vectors corresponding to the respective interrupt vectors is stored in the second storage area (col. 8, lines 22-25; Fig. 8, elements (30-1)~(30-n));

a central processing unit that has a mechanism to access the nonvolatile memory (col. 3, lines 19-23 and 28-29; Fig. 1, element 2).

Yamada does not expressly disclose a flag indicating that the first storage area is not accessible;

and a conversion circuit that includes a register to which an offset is set, and that converts a first address indicating a storage place of the interrupt vector that is accessed by the central processing unit into a second address indicating a storage place of the corresponding alternate interrupt vector by adding the offset to the first address.

Iwata discloses a flag indicating that the first storage area is not accessible (col. 9, lines 51-55 and 58-61; col. 10, lines 50-58; Fig. 1, element 18); *See the citation note for the similar limitation in claim 1 above.*

and a conversion circuit that includes a register, and that converts a first address indicating a storage place of the interrupt vector that is accessed by the central processing unit into a second address indicating a storage place of the corresponding alternate interrupt vector (col. 14, lines 6-15; col. 23, line 60; Fig. 5; Fig. 19).

Yamada and Iwata are analogous because they are from the same field of endeavor, that being microcomputers.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Iwata's conversion circuit within Yamada's microcomputer.

The motivation for doing so would have been to improve the safety of a system during on-board programming of a program memory (Iwata, col. 3, lines 25-27). Also, another motivation for doing so would have been to provide additional safety by preventing a microcomputer from running away and from being damaged even when an interrupt handling or exception handling is requested during on-board programming of the above program memory (Iwata, col. 3, lines 31-34).

The combination of Yamada/Iwata does expressly disclose a conversion circuit that includes a register to which an offset is set, and that converts a first address indicating a storage place of the interrupt vector that is accessed by the central processing unit into a second address indicating a storage place of the corresponding alternate interrupt vector by adding the offset to the first address.

Yoshioka discloses a register to which an offset is set, that adds the offset to the first address (col. 15, lines 17-26; col. 17, lines 23-31; Fig. 14). *It should be noted that the "shifter" is a form of a shift register.*

The combination of Yamada/Iwata and Yoshioka are analogous because they are from the same field of endeavor, that being microcomputers.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Yoshioka's vector offset hardware within Yamada/Iwata's microcomputer.

The motivation for doing so would have been to make it possible to accomplish both a reduction in the physical scale of the circuit and an increase in the data processing speed (Yoshioka, col. 24, lines 60-63).

Therefore, it would have been obvious to combine Yamada, Iwata, and Yoshioka for the benefit of obtaining the invention as specified in claim 28.

27. Claim 18 is rejected under 35 U.S.C. 103(a) as being obvious over Yamada in view of Iwata as applied to claim 15 above, and further in view of Andrew S. Tanenbaum, Structured Computer Organization, 2nd Edition, hereafter "Tanenbaum."

28. The combination of Yamada/Iwata discloses the conversion circuit performs a predetermined conversion operation based on a setting by a hardware (Iwata, col. 14, lines 36-54; Fig. 5). *It should be noted that the conversion is performed based on the settings of the logic circuits and selection circuits (i.e. hardware).*

The combination of Yamada/Iwata does not expressly disclose the conversion circuit performs a predetermined conversion operation based on a setting by a software.

Tanenbaum discloses that hardware and software are logically equivalent (pg. 11, line 11).

The combination of Yamada/Iwata and Tanenbaum are analogous art because they are from the same field of endeavor, that being computer systems design.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to follow Tanenbaum's argument and base Yamada/Iwata's conversion operation on software settings.

The motivation for doing so would have been to optimize such factors as cost, speed, and reliability (Tanenbaum, pg. 11, lines 14-15).

Therefore, it would have been obvious to combine Yamada/Iwata and Tanenbaum for the benefit of obtaining the invention as specified in claim 18.

29. Claim 5 is rejected under 35 U.S.C. 103(a) as being obvious over Yamada in view of Iwata and further in view of Hashimoto as applied to claim 1 above, and further in even view of Tanenbaum.

30. The combination of Yamada/Iwata/Hashimoto discloses the conversion circuit performs a predetermined conversion operation based on a setting by a hardware (Iwata, col. 14, lines 36-54; Fig. 5). *It should be noted that the conversion is performed based on the settings of the logic circuits and selection circuits (i.e. hardware).*

The combination of Yamada/Iwata/Hashimoto does not expressly disclose the conversion circuit performs a predetermined conversion operation based on a setting by a software.

Tanenbaum discloses that hardware and software are logically equivalent (pg. 11, line 11).

The combination of Yamada/Iwata/Hashimoto and Tanenbaum are analogous art because they are from the same field of endeavor, that being computer systems design.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to follow Tanenbaum's argument and base Yamada/Iwata/Hasimoto's conversion operation on software settings.

The motivation for doing so would have been to optimize such factors as cost, speed, and reliability (Tanenbaum, pg. 11, lines 14-15).

Therefore, it would have been obvious to combine Yamada/Iwata/Hashimoto and Tanenbaum for the benefit of obtaining the invention as specified in claim 5.

31. Claims 26-27 are rejected under 35 U.S.C. 103(a) as being obvious over Yamada in view of Iwata as applied to claims 20-21, and further in view of Fudeyasu et al. (U.S. Patent 6,154,837).

32. **As per claims 26-27**, the combination of Yamada/Iwata discloses all the limitations of claims 26-27 except a main program is stored in a memory other than the nonvolatile memory.

Fudeyasu discloses a main program is stored in a memory other than the nonvolatile memory (col. 3, lines 37-41; col. 4, lines 25-28; Fig. 1, elements 2 and 4). *It should be noted that "boot ROM" is analogous to "nonvolatile memory."*

The combination of Yamada/Iwata and Fudeyasu are analogous art because they are from the same field of endeavor, that being interrupt processing within microcomputers.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Fudeyasu's RAM within Yamada/Iwata's microcomputer.

The motivation for doing so would have been to offer the advantage of being able to provide a microcomputer that can achieve effective interrupt processing in boot mode by enabling an erase/write program to execute interrupt processing freely (Fudeyasu, col. 5, lines 5-9).

Therefore, it would have been obvious to combine Yamada/Iwata and Fudeyasu for the benefit of obtaining the inventions as specified in claims 26-27.

33. Claims 13-14 are rejected under 35 U.S.C. 103(a) as being obvious over Yamada in view of Iwata and further in view of Hashimoto as applied to claims 7-8, and in even further view of Fudeyasu et al. (U.S. Patent 6,154,837).

34. **As per claims 13-14**, the combination of Yamada/Iwata/Hashimoto discloses all the limitations of claims 13-14 except a main program is stored in a memory other than the nonvolatile memory.

Fudeyasu discloses a main program is stored in a memory other than the nonvolatile memory (col. 3, lines 37-41; col. 4, lines 25-28; Fig. 1, elements 2 and 4). *See citation note for claims 26-27 above.*

The combination of Yamada/Iwata/Hashimoto and Fudeyasu are analogous art because they are from the same field of endeavor, that being interrupt processing within microcomputers.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Fudeyasu's RAM within Yamada/Iwata/Hasimoto's microcomputer.

The motivation for doing so would have been to offer the advantage of being able to provide a microcomputer that can achieve effective interrupt processing in boot mode by enabling an erase/write program to execute interrupt processing freely (Fudeyasu, col. 5, lines 5-9).

Therefore, it would have been obvious to combine Yamada/Iwata/Hashimoto and Fudeyasu for the benefit of obtaining the inventions as specified in claims 13-14.

Response to Arguments

35. Applicant's arguments filed in the communication dated July 19, 2006 with respect to **claims 1 and 4-27** have been fully considered but they are not persuasive.

36. With respect to Applicant's argument in fourth full paragraph of page 8 of the communication filed July 19, 2006, the Examiner respectfully disagrees and refers Applicant to the rejection of claim 1 above. The Examiner would also like to specifically

refer Applicant to Iwata col. 23, lines 60-63 and Fig. 19, which discloses registers PEREG, MBREG1, and MBREG2 (i.e. "a plurality of registers").

37. With respect to Applicants argument in the fifth full paragraph of page 8 of the communication filed July 19, 2006 that "There is no adequate motivation to combine the microcomputer of Yamada with the data processor of Iwata without having to rely on Applicant's own disclosure..." the Examiner respectfully disagrees. In response to applicant's argument that the Examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

38. With respect to Applicant's argument in the sixth full paragraph of page 8 into page 9 of the communication filed July 19, 2006, the Examiner respectfully disagrees and refers Applicant the rejection of claim 15 above. The Examiner would also like to specifically refer Applicant to Iwata col. 23, lines 60-63 and Fig. 19, which discloses registers PEREG and MBREG1 ("a first pair of registers") and registers PEREG and MBREG2 ("a second pair of registers").

39. As for Applicant's arguments with respect to dependent claims 4-14 and 16-27, the arguments rely on the allegation that independent claims 1 and 15 should be allowable and therefore for the same reasons dependent claims 4-147 and 16-27

should be allowable. However, as addressed above, independent claims 1 and 15 are not patentably distinct over the cited prior, thus, Applicant's arguments with respect to dependent claims 4-147 and 16-27 are not persuasive.

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, **claims 1 and 4-29** have received a second action on the merits and are subject of a second action final.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Arpan Savla
Art Unit 2185
September 26, 2006

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